USN | | | | | | | | | | |

10EC021

M.Tech. Degree Examination, June/July 2011
CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Describe the working of nMOS enhancement mode transistor, with a neat sketches and sketches and output characteristics. **(08 Marks)**

b. Briefly explain the second order effects in MOSFETS. **(06 Marks)**

c. Describe the working of differential inverter with transfer characteristics. **(06 Marks)**

2 a. Explain the transmission gate output characteristics for change in control input and for change in switched input. **(06 Marks)**

b. Calculate the native threshold voltage for an n – transistor at 300°K for a process with a silicon substrate with $N_A = 1.8 \times 10^{16}$/cc, $t_{ox} = 200$°A. Assume $\phi_{ms} = 0.9$ V, $\varphi_{fc} = 0$, $n_1 = 1.45 \times 10^{16}$/cc. **(06 Marks)**

c. With neat sketches, explain the working principle of static load Pseudo – nMOS inverter. **(08 Marks)**

3 a. Explain the fabrication of silicon on insulator (SOI) CMOS process technology. List the advantages of SOI process. **(10 Marks)**

b. Obtain the scaling factors for following : i) Power dissipation per gate P_g
ii) Saturation current Idss. **(05 Marks)**

c. A MOS layer is 6λ wide, 60λ long and 1μm thick. The resitivity of the layer is 1Ω cm, using a sheet resistance concept, calculate the total resistance of the MOS layer along its length. **(05 Marks)**

4 a. Explain λ - based design rules as applicable to MOS layers and transistors. **(08 Marks)**

b. Draw the CMOS circuit diagram and stick diagram for a 2 input Nand gate. **(04 Marks)**

What is latch-up problem? with neat sketch, explain the occurrence of a latch – up problem.

c. List the remedies to avoid the latch – up problem. **(08 Marks)**

5 a. Derive the threshold voltage equation (Vt) for 2 input NOR gate. **(10 Marks)**

b. For the given function $f = \overline{A}B + A\overline{B}$, obtain : i) CMOS te realization
ii)CMOS transistor realization. **(06 Marks)**

c. Explain the AND – OR – Inverter (AOI) and OR – AND – Inverter (OAI) logic, with suitable example. **(04 Marks)**

6 a. With circuit diagram, explain the working of clocked SR latch. **(06 Marks)**

b. Explain the operation nMOS pass transistor with charge storage and charge leakage capabilities. **(08 Marks)**

c. Draw the CMOS logic circuit for the function $\overline{(D+E+A)(B+C)} = f$ **(06 Marks)**

7 a. With qualitative analysis, explain the operation of basic differential amplifier and derive the equation for voltage gain Av. **(12 Marks)**

b. Write a short note on band – gap references. **(08 Marks)**

8 a. How domino CMOS logic is formed? Describe the operation of NORA CMOS logic. **(10 Marks)**

b. Bring out the differences between ratioed logic and ratioless logic, with respect to 3-bit shift register. **(10 Marks)**

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